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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/066,188	
	Filing Date	1/31/02	
	First Named Inventor	Steven Teig, et al.	
	Group Art Unit	2661	
	Examiner Name	<none yet>	
Total Number of Pages in This Submission	*	Attorney Docket Number	SPLX.P0095

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Date	January 16, 2004

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PATENT
Docket No. SPLX.P0095

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Mani Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/066,188

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
SPECIFYING ENCODED SUB-NETWORKS

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Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.


This Information Disclosure Statement is submitted within three months of the application filing date or before the mailing date of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

If the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing **SPLX.P0095**. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

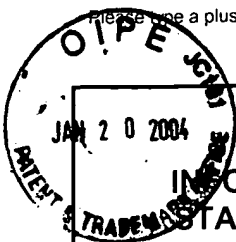
Dated: January 16, 2004

Respectfully submitted,

By: 
Mari Adeli
Registration No. 39,585

Stattler, Johansen & Adeli LLP
P.O. Box 51860
Palo Alto, CA 94303-0728

Phone No. (650) 752-0990 x102
Fax No. (650) 752-0995

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	2	Application Number	10/066,188
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2661
				Examiner Name	
				Attorney Docket Number	SPLX.P0095

U.S. PATENT DOCUMENTS

Examiner* Initials	Cite No. ¹	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
	4.	4,703,435		10-27-1987	Darringer et al.	
	5.	5,003,487		03-26-1991	Drumm et al.	
	6.	5,537,330		07-16-1996	Damiano et al.	
	7.	5,892,678		04-06-1999	Tokunoh et al.	
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	11.	6,311,317	B1	10-30-2001	Khoche et al.	
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	20.	6,543,037	B1	04-01-2003	Limqueco et al.	
	21.	6,546,541	B1	04-08-2003	Petranovic et al.	

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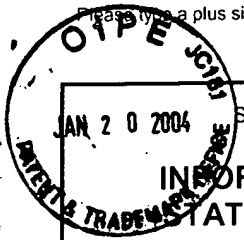
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/066,188
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2661
				Examiner Name	
Sheet	2	of	2	Attorney Docket Number	SPLX.P0095

U.S. PATENT DOCUMENTS

22.	6,618,835	B1	09-09-2003	Garlapati et al.
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NON PATENT LITERATURE DOCUMENTS

Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	23.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).	
	24.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vol. 37, No. 11, pp. 291-292 (4 pages).	
	25.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.	
	26.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.	
	27.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.	

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